REMARKS

Claims 25, 31 have been amended. Support for the amendment of Claims 25, 31 appears in the specification at least at page 15, lines 23-30 and in FIGS. 1, 7. Claim 33 has been amended for purposes of clarity.

Claims 25-33 are patentable over Kinsman (6,172,419) in view of Akram et al. (6,313,522).

Regarding Kinsman, the Examiner states:

> Kinsman discloses a semiconductor package with (25) a **substrate (102) having a first surface, an opposite second surface,** and central throughhole between the first and second surfaces; ... **a semiconductor chip (120)** in said throughhole ... **wherein ... the second surface of the semiconductor chip (120) is flush with the second surface of the substrate;** (Office Action, pages 2-3, emphasis added.)

However, Kinsman teaches that the "second surface" of "the semiconductor chip (120)" is mounted to a thin sheet material 116. Thus, the Examiner has failed to callout where Kinsman teaches or suggests that the "second surface" of "the semiconductor chip (120)" is exposed.

Specifically, Kinsman teaches:

> An upward facing cavity is formed by securing a support base such as thin sheet material 116 to the bottom of substrate 102 to cover aperture 114. ... The dimensions (length and width) of the thin sheet material 116 are greater than the dimensions (length and width) of aperture 114 so as to completely cover aperture 114, but typically less than the dimensions (length and width) of substrate 102. BGA package 100 further comprises a **semiconductor element or die 120 mounted in the cavity formed by the aperture 114 and thin sheet material 116**, which minimizes the effect of die thickness on the overall package height. (Col. 4, line 50 to Col. 5, line 2, emphasis added.)

Akram et al. does not cure the deficiency in Kinsman.

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Specifically, in reference to FIG. 5, Akram et al. teaches:

> In the illustrated embodiment of FIG. 5, **the interconnect devices 51, 52, 53 function to provide a structural interface for the semiconductor devices 20, 22, 24, respectively**. The interconnect devices 51, 52, 53 may comprise a flex circuit without any conductive wires, and thus, is non-conductive, or a flex circuit in which there is no electrical connection with the conductive wires. **The interconnect devices 51, 52, 53 are coupled to the substrates 14, 16, 18, respectively, using an appropriate adhesive 60 or other suitable fastening means.**
>
> **The semiconductor devices 14, 16, 18 are mounted on the interconnect devices 51, 52, 53, respectively, using an appropriate adhesive 62** or other suitable semiconductor fastening means, such that the semiconductor devices 14, 16, 18 are positioned within respective openings 14D, 16D, 18D of the respective substrates 14, 16, 18. (Col. 12, line 7 to line 22, emphasis added.)

Accordingly, Akram et al. teaches that the lower surfaces of the semiconductor devices 20, 22, 24 are mounted on the interconnect devices 51, 52, 53, respectively. Thus, Kinsman and Akram et al., either alone or in combination, do not teach or suggest:

> A stackable semiconductor package comprising:
>
> a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;
>
> a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;
>
> a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first

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surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and **the second surface of the semiconductor chip is flush with the second surface of the substrate, wherein the second surface of the semiconductor chip is exposed**; and

a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant,

as recited in amended Claim 25, emphasis added. Accordingly, Claim 25 is allowable over Kinsman in view of Akram et al. Claims 26-30, which depends from Claim 25, are allowable for at least the same reasons as Claim 25.

Claim 31 is allowable for reasons similar to Claim 25. Claims 32-33, which depends from Claim 31, are allowable for at least the same reasons as Claim 31.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 25-33 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 30, 2006.

Attorney for Applicant(s) — May 30, 2006 Date of Signature

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